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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,337	PRITCHARD ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/28/06 & 6/16/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 18-25* is/are pending in the application.

4a) Of the above claim(s) *1-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed February 28, 2006 and Election filed June 16, 2006, in which claims 18-25 are elected, without traverse. Claims 1-15 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention. Claims 16-17 were cancelled.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Objection

1. Claims 24-25 are objected for lacking antecedent basis and/or including typographical errors.

** In claim 25, at line 5, the phrase "...a source, and a gate..." should be --...a source, and a drain...-- (see line 6 for "the drain").

** In claim 24, the phrase --the strained silicon substrate implant..." is lacking antecedent basis, and should be --the epitaxially grown silicon layer-- as mentioned in claim 21.

Claim Rejections - 35 USC § 103

2. Claims 18,19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sing et al (6,645,818) taken with Inumiya (6,054,355).

Sing teaches a method of forming a semiconductor integrated circuit, the method comprising: providing a substrate comprised of semiconductor material 10 having isolation structures 12 formed thereon, the substrate exposing the semiconductor material 16 having a planar surface located above the N-well region 16 so that the isolation structures 12 define exposed transistor forming regions of the substrate surface (Fig 1; col 2, lines 56-65); forming source and drain diffusion regions 34 in exposed transistor forming regions of the substrate surface (Fig 4; col 3, lines 13-17); annealing the semiconductor substrate (col 3, lines 18-24); after forming the source and drain diffusion regions 34 and after annealing, covering the surface of the semiconductor substrate with a first layer 76 (Fig 13; col 4, lines 45-52) of dielectric material to form a first interlayer dielectric layer 76 on the semiconductor substrate after formation of the source and drain diffusions 34; etching a gate electrode trench (Fig 13) in the interlayer dielectric layer 76 (col 4, lines 53-57), the gate electrode trench configured for the

placement of a transistor gate electrode 84/86 between the source and drain regions 34; lining the gate electrode trench with a high-K dielectric film 82 (Fig 14; col 4, lines 58-65); and depositing a gate electrode 86/84 conductive material in the gate electrode trench after lining the trench with the high-K dielectric film 82 (Fig 14-15; col 4, line 58 through col 5).

Re claim 18, Sing already teaches providing the substrate 10 comprised of semiconductor material having isolation structures 12 (as shown in Figure 1). Claim 18 recites the substrate having a planarized surface.

Although, as shown in Figure 1 of Sing, the substrate 10 having isolation structures 12 appears to have a planar surface, Inumiya further teaches (at Figs 52B-58; col 36, line 30 through col 37; Figs 40A-40B; col 23, line 65 through col 24, line 8;) forming a substrate (61 in Fig 52B; 401 in Fig 40A) comprised of semiconductor material having isolation structures (62 in Fig 52B; 402 in Fig 40A), wherein the substrate 61,401 is formed to have a planarized surface by planarization (Fig 52B, 40A, col 24, lines 1-8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor device of Sing by providing the substrate having a planarized surface by planarization as taught by Inumiya. This is because of the desirability to increase the planarized surface area of the substrate so as to form a planarized semiconductor device, thereby forming a thinner and miniaturized planar semiconductor device.

Re claims 19-20, Sing does not teach forming a trench extension into the substrate (claim 19); and Re claim 20, the trench has a depth to include an entire device inversion channel.

However, Inumiya further teaches (at Figs 53-58, col 37, lines 20-42; Figs 60A-61B; col 41, lines 15-28; Figs 65A-65C, col 43, line 43 through col 44) etching the gate electrode trench in the first dielectric layer 66 to form a trench extension that extends into the substrate 61 (Figs 53B,54,,58,65A-65C), wherein the trench extension extends into the substrate a depth sufficient to include an entire device inversion channel for the integrated circuit device (as shown in Figs 53B,54,,58,65A-65C).

Therefore, it would have been also obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit device of Sing by forming form a trench extension that extends into the substrate to a depth sufficient to include an entire device inversion

channel for the integrated circuit device, as taught by Inumiya. This is because of the desirability to buried the gate electrode in the trench recessed in the substrate thereby improving planarization of the semiconductor device, and because of the desirability to increase thickness of the gate electrode, thereby reducing wiring resistance, and thereby improving driving speed performance of the semiconductor device.

3. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sing et al (6,645,818) taken with Inumiya (6,054,355), as applied to claims 18-20 above, and further of Dakshina-Murthy (6,406,950).

The references including Sing and Inumiya teach a method of forming a semiconductor integrated circuit as applied to claims 18-20 above. Re claim 25, Sing also already teaches covering the surface of the semiconductor substrate with a second layer 90 of dielectric material (Fig 16; col 5, lines 10-20); forming at least one opening in the first and second layers 90,76 of dielectric materials to expose at least one of the source/drain regions; depositing a conductive material in the at least one opening to electrically contact the salicide 50 formed on the exposed at least one of the source/drain; and removing excess conductive material.

The references including Sing thus lack forming the opening to expose the source/drain region and forming a salicide on the exposed source/drain regions and planarization to remove excess conductive material (re claim 25).

However, Dakshina-Murthy teaches (at Figures 11-12; col 7, lines 11-26) a process by forming the opening to expose the source and drain regions; forming a salicide 98 (Fig 11) on the exposed source/drain regions 36,38,60,62; and planarization to remove excess conductive material 102 (col 7, lines 11-26; Fig 12), wherein the process comprises covering the surface of the semiconductor substrate with a second layer 94 of dielectric material (Figs 11-12,10; col 7, lines 11-26); forming at least one opening in the first and second layers 94,34 of dielectric materials to expose at least one of a gate electrode, a source, and a drain; forming a salicide 98 on the exposed at least one of the source and the drain (Fig 11, 36,38,60,62); depositing a conductive material 102 in the at least one opening to electrically contact the salicide formed on the exposed at least one of the source and the drain (Fig 12); and planarizing the surface to remove excess conductive material.

Therefore, it would have been also obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit device of the references including Sing by forming a salicide on the exposed source and drain regions, and planarizing to remove excess conductive material as taught by Dakshina-Murthy. This is because of the desirability to form the salicide on the source and drain regions in a self-alignment manner with respect to the exposed opening, whereby the salicide reduces sheet resistance, and because of the desirability to form a planarized semiconductor device by planarizing to remove excess conductive material.

4. Claims 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sing et al (6,645,818) taken with Inumiya (6,054,355), as applied to claims 18-20 above, and further of Sugawara (6,750,486) and Hammond et al (6,680,496).

The references including Sing and Inumiya teach a method of forming a semiconductor integrated circuit as applied to claims 18-20 above.

Re claims 21-24, The references including Sing and Inumiya lacks epitaxially growing a strained silicon layer formed on a SiGe layer in the trench.

However, Sugawara teaches (at Figs 2-4;1; col 4, line 57 through col 6) epitaxially growing an Ge-containing layer including SiGe layer on the channel trench, and a silicon layer thereon. Hammond also teaches (at Figs 3A-3B; col 6, line 40 through col 7; col 10, lines 46-61) epitaxially growing a strained silicon layer formed on a SiGe layer or Ge layer grown in the channel.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Inumiya by epitaxially growing a strained silicon layer formed on a SiGe layer or Ge layer grown in the channel, as taught by Sugawara and Hammond. This is because to enhance high mobility electron or hole channel in strained device.

Response to Amendment

5. Applicant's arguments filed Feb 28, 2006 with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oacs-18

Michael Trinh
Primary Examiner